REMARKS

Claims 1 - 4 and 6 - 15 remain active in this application. The indication of claims 13 - 15 as being drawn to allowable subject matter is noted with appreciation. No amendments are currently requested and mo new matter has been introduced into the application.

Claims 1 - 2 and 6 - 12 have been rejected under 35 U.S.C. §102 as being anticipated by U.S. Patent 5,740,391 to Hunt (hereinafter "Hunt"). Claims 3 - 4 have been rejected under 35 U.S.C. §103 as being unpatentable over Hunt. These grounds of rejection are respectfully traversed for the reasons of record, and in view of the remarks below.

As discussed in the previous responses of record, the present invention is directed to an instruction buffer and a method for controlling an instruction buffer, particularly for a processor having a pipelined architecture such that several instructions can be processed simultaneously, either in-order or out-of-order.

With regard to the rejection of claims 1 - 4 and 6 - 15 under 35 U.S.C. §102, MPEP 2131 expressly states that "to anticipate a claim, the reference must teach <u>every element</u> in the claim" (emphasis added). Further, MPEP 2131, citing <u>Richardson v. Suzuki Motor Co.</u>, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989), states "[t]he identical invention must be shown in as complete detail as is contained in the . . . claim." As Hunt teaches a system and method that minimizes additional logic required to track early exception conditions in a microprocessor system, as well as eliminating premature false signaling of exceptions (see column 3, lines 35-54, in Hunt), it is respectfully submitted that the Examiner has failed to establish his *prima facie* burden under 35 U.S.C. §102.

With regard to claim 1, and dependent claims 2-4, of the present invention, Hunt clearly does not answer the recitation of first and second buffers wherein <u>each issues instructions in storage entry order</u>. While it appears that Hunt may teach separate but serially connected buffer units (342, 344 in Figure 3 in Hunt), and may preclude a parallel path/pipeline for out-of-order execution, Hunt fails to teach or contemplate <u>any</u> difference in order of instructions in the <u>single</u>

instruction buffer. In fact, Hunt only teaches the insertion of instructions into the single instruction buffer 316 and removal from the same buffer in the same order of entry (see column 7, lines 47-54, in Hunt) for the purpose of preventing premature exception signaling when the buffer management unit 328 encounters a mispredicted branch instruction. Therefore, it is respectfully submitted that Hunt does not anticipate claim 1, nor dependent claims 2-4, of the present invention and the ground of rejection based on Hunt under 35 U.S.C. §102 is untenable in regard to the claims.

With regard to claims 6-10 of the present invention, claim 6 emphasizes that while one instruction in the second group of instructions is executed, other instructions in the first group of instructions are contemporaneously executed. Hunt clearly fails to teach or suggest such a method for controlling a buffer queue where instructions in two different groups are executed at the same time. Therefore, it is respectfully submitted that Hunt does not anticipate claim 6, nor dependent claims 7-10, of the present invention and the ground of rejection based on Hunt under 35 U.S.C. §102 is untenable in regard to the claims.

With regard to claims 11-15 of the present invention, Hunt clearly teaches only one instruction buffer and one order for instructions issued (see column 7, lines 41-42, in Hunt - "...the retire unit 322 *must* remove instructions from the instruction buffer 316 *in program order.*") (emphasis added). Furthermore, the instructions in Hunt are merely sorted between the ALU instruction buffer 410 and the memory access buffer 420, but are still "retied" in FIFO manner (see column 7, lines 54-57, and Figure 4 in Hunt). Therefore, it is respectfully submitted that Hunt does not anticipate claim 11, nor dependent claims 12-15, of the present invention and the ground of rejection based on Hunt under 35 U.S.C. §102 is untenable in regard to the claims. Accordingly, it is respectfully requested that the ground of rejection based on Hunt with regard to claims 11-15 be reconsidered and withdrawn and the application be passed to issue.

In regard to the separate rejection of claims 3 and 4, the Examiner relies on the propriety of the rejection of claim 2 which has been demonstrated above to be incorrect and improper. The Examiner then admits that Hunt does not answer the recitations of claims 3 and 4 but takes official notice that the entirety of the further recitations of claim 3 and 4 are conventional without

any evidence thereof other than a citation of column 7, line 35 of Hunt. This recitation (continuing through line 38) essentially indicates that any workable method for launching instructions can be used "so long as the retire unit 322 *removes* the instructions from the instruction buffer 213 *in program order*" (emphasis added) which has nothing to do with "the instruction first issued from among the entries of the first buffer *whose instructions are ready to be issued* is the entry *having a lowest entry number among said entries of the first buffer whose instructions are ready to be issued*" (claim 3 - emphasis added) or "wherein the entries of the first buffer storing the instructions *are lower in entry number than* the *entries storing no instructions*" (claim 4, emphasis added). The Examiner's position appears to be that it would be conventional to issue instructions *in program order* and such may well be the case. However, the invention as recited in claims 1 - 4 is directed to provision of the capability of issuing instructions in order *or out of order* (to improve efficiency of instruction issuance and utilization of high-speed processing hardware such as ALUs - see paragraph bridging pages 1 and 2) while avoiding the problem of filling the instruction buffer with instructions which are waiting for results of instructions which have not been issued which is commonly encountered when instructions are issued out of program order. Clearly the Examiner's rationale, as stated, is logically flawed in regard to the actual recitations of claims 3 and 4 and does not address the actual recitations of the claims (e.g. considering instructions which are *ready* to be issued or the relative order of entry numbers between entries which contain instructions and those which do not) but is, in fact, contrary thereto as well as the ultimate meritorious function(s) supported by those recitations. Moreover, it is respectfully submitted to be improper to take official notice of conventionality of the *entirety* of any claim, even if the claim is dependent from another claim (assuming the Examiner's assertion to be so limited). Therefore, it is respectfully submitted that the rejection of claims 3 and 4 is improper and clearly in error on its face and thus untenable and that the Examiner has not made a *prima facie* demonstration of obviousness of any claim and cannot do so, particularly in view of the Examiner's admissions in regard to these claims. Accordingly it is respectfully requested that the rejection of claims 3 and 4 be reconsidered and withdrawn.

Since all rejections, objections and requirements contained in the outstanding official action have been fully answered and shown to be in error and/or inapplicable to the present claims, it is respectfully submitted that reconsideration is now in order under the provisions of 37 C.F.R. §1.111(b) and such reconsideration is respectfully requested. Upon reconsideration, it is also respectfully submitted that this application is in condition for allowance and such action is therefore respectfully requested.

If an extension of time is required for this response to be considered as being timely filed, a conditional petition is hereby made for such extension of time. Please charge any deficiencies in fees and credit any overpayment of fees to Attorney's Deposit Account No. 50-2041.

Respectfully submitted,

Marshall M. Curtis

Marshall M. Curtis
Reg. No. 33,138

Whitham, Curtis & Christofferson, P. C.
11491 Sunset Hills Road, Suite 340
Reston, Virginia 20190

Customer Number: **30743**

(703) 787-9400